Toward real-time multiscale brain modeling on iono-neuromorphic silicon neuron chips

Chi-Sang Poon

Harvard-MIT Division of Health Sciences and Technology,
Massachusetts Institute of Technology

June 11, 2012
(Monday)
10 am

Seminar Room 1
(#01-06)
Center for Life Sciences
(CeLS)
28 Medical Drive
National University of Singapore
Singapore 117456

Neural modeling in current literature relies heavily on computer simulation “in silico”. However, even today’s supercomputers cannot simulate large-scale brain networks in real time. Biological neurons excel in performing massive analog computations in parallel at minute power consumption within a tiny anatomic space while neuron-to-neuron communication is predominantly digital via all-or-none spiking. Neuromorphic silicon neurons fabricated on very-large-scale integrated (VLSI) circuits with complementary metal-oxide-semiconductor (CMOS) transistor technology allow neuronal spiking dynamics to be directly emulated on silicon chips with much better power and space efficiencies and computing speed than digital simulation. Iono-neuromorphic silicon neurons go even further in mimicking not only neuronal spiking dynamics at the network level but also ion channel and intracellular ionic dynamics at the cellular level. Such iono-neuromorphic silicon neuron networks offer a highly efficient computational platform that is particularly well-suited for multiscale biophysically-based neural computing in real time under stringent power and space/weight constraints, with potential applications in cognitive neuroprosthesis, brain–computer interface, and embedded machine intelligence devices. In this talk, I will discuss: 1) recent advances in iono-neuromorphic silicon neuron modeling of various complex neuronal dynamics including chaotic pacemaker bursting, single-neuron mnemonics with long-lasting persistent activity, and spike-rate-dependent/spike-timing-dependent plasticity with retrograde endocannabinoid signaling; 2) challenges facing large-scale iono-neuromorphic computation on CMOS silicon chips and other nanodevices; 3) recent advances in ultralow-power and three-dimensional CMOS technology that will empower the next generation of large-scale iono-neuromorphic silicon neuron networks and applications.

Chi-Sang Poon received the Ph.D. degree from the University of California, Los Angeles. He was Visiting Scientist at Biologie Fonctionnelle du Neurone, CNRS, France, in 1994. He is presently Principal Research Scientist, Harvard-MIT Division of Health Sciences and Technology, Massachusetts Institute of Technology, Cambridge. His main research areas include neurophysiology and neuroengineering. He has also made many contributions in signal processing, systems biology, and social sciences. He is on the editorial boards of the journals Frontiers in Neuromorphic Engineering and Behavioral and Brain Functions. Dr. Poon is an Inaugural Fellow of Biomedical Engineering Society (BMES).